

# Blue Pearl Software 사 Analyze RTL

**A. 목적** : Lowers Design Risk and improves Quality of Results (QoR)

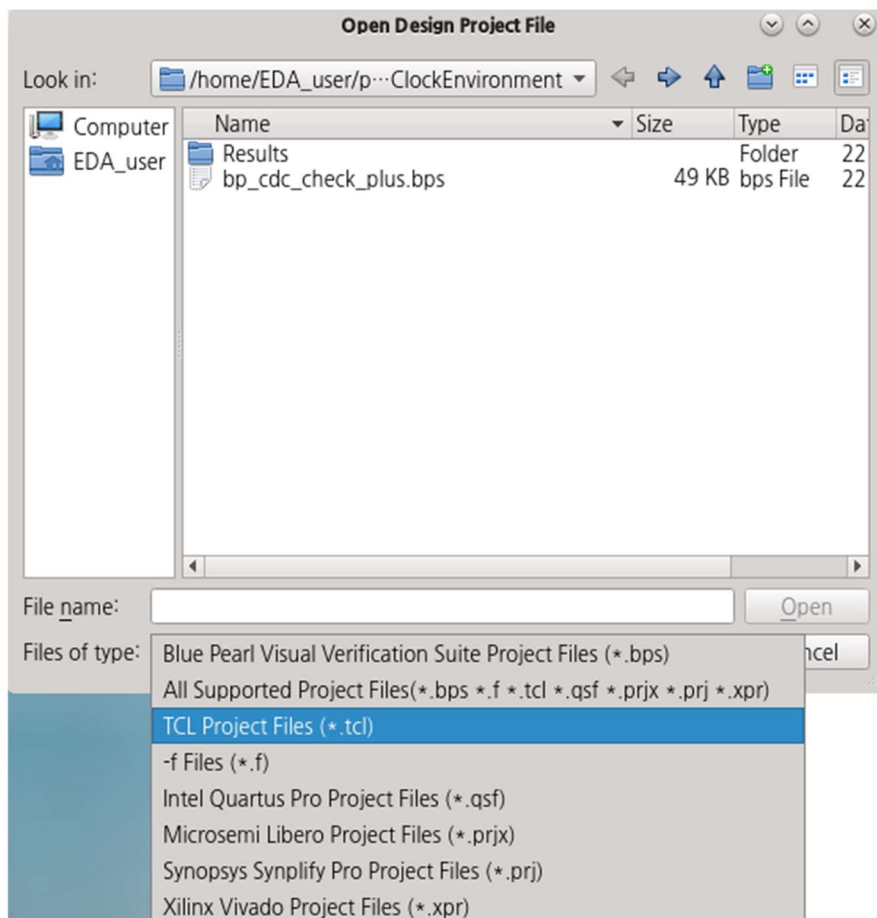
**B. 구분** : Functional Design Analysis to verify properties, methodology standards and design rules

**C. Supported Platform and O/S System**

- RHEL 6, 7, 8 (64 bit)
- Windows 7, 8.1, 10 (64 bit)

**D. 특성 및 기능**

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- IEEE Verilog / Systemverilog / VHDL 표준에 맞는 Syntax Check 진행
- 3<sup>rd</sup> Party Tool (Xilinx Vivado, Intel Quartus, Microsemi Libero)의 Project 파일과의 호환성 제공
- 다양한 Built-in Rule을 이용하여 Custom한 검증 환경 구성 가능 (Naming Convention 등에 대한 Built-in Check, DO-254 표준 Check 및 3<sup>rd</sup> Party Tool과의 호환성 Check 등)
- RTL Code와 Schematic 간의 Cross-probing 등의 Graphical Analysis 지원



3<sup>rd</sup> Party Tool 의 Project 파일과의 호환성 제공

Group by:  
 Packages  Ungrouped

Filter...

Hide Un-checked items?  Hide Un-licensed items?

<ul style="list-style-type: none"><li>▶ <input checked="" type="checkbox"/> Bad Logic</li><li>▶ <input checked="" type="checkbox"/> Basic Checks</li><li>▶ <input type="checkbox"/> Low Power</li><li>▶ <input checked="" type="checkbox"/> Design initializes/resets</li><li>▶ <input checked="" type="checkbox"/> No Races</li><li>▶ <input checked="" type="checkbox"/> No redundant logic</li><li>▶ <input checked="" type="checkbox"/> No drive conflicts</li><li>▶ <input checked="" type="checkbox"/> No X-source problems</li><li>▶ <input type="checkbox"/> Clocks</li><li>▶ <input type="checkbox"/> Clock Domain Crossings</li><li>▶ <input checked="" type="checkbox"/> Advanced Clock Environment<ul style="list-style-type: none"><li>▶ <input checked="" type="checkbox"/> CLOCK_RECOMMENDATIONS - Make recommendations regarding...</li></ul></li><li>▶ <input type="checkbox"/> Coding style</li><li>▶ <input checked="" type="checkbox"/> Coding conventions</li><li>▶ <input checked="" type="checkbox"/> Assignment Checks</li><li>▶ <input checked="" type="checkbox"/> Simulation/Synthesis</li><li>▶ <input checked="" type="checkbox"/> No implied_latches</li><li>▶ <input checked="" type="checkbox"/> Case statements</li><li>▶ <input checked="" type="checkbox"/> No size conflicts</li><li>▶ <input checked="" type="checkbox"/> Naming</li><li>▶ <input type="checkbox"/> Signal Identification</li><li>▶ <input type="checkbox"/> Comments</li><li>▶ <input checked="" type="checkbox"/> FSM Checks</li><li>▶ <input checked="" type="checkbox"/> Miscellaneous checks</li><li>▶ <input type="checkbox"/> SDC Verification</li><li>▶ <input checked="" type="checkbox"/> Cycle Based Simulation</li><li>▶ <input type="checkbox"/> VHDL Only</li><li>▶ <input checked="" type="checkbox"/> Input IP</li><li>▶ <input checked="" type="checkbox"/> New RTL</li><li>▶ <input checked="" type="checkbox"/> Golden RTL</li><li>▶ <input checked="" type="checkbox"/> DFT</li><li>▶ <input checked="" type="checkbox"/> Principles of Verifiable RTL</li><li>▶ <input checked="" type="checkbox"/> Reuse Methodology Manual</li><li>▶ <input checked="" type="checkbox"/> Semiconductor Reuse Standard</li><li>▶ <input checked="" type="checkbox"/> DO-254</li><li>▶ <input checked="" type="checkbox"/> STARC</li><li>▶ <input checked="" type="checkbox"/> UltraFast Design Methodology for Vivado</li><li>▶ <input checked="" type="checkbox"/> Quartus II Best Practices</li><li>▶ <input checked="" type="checkbox"/> Microsemi RTG4 Best Practices</li></ul>	<h3>Package: DO-254</h3> <p><b>Description:</b> This package includes checks that aid in compliance with the DO-254 military standard.</p> <p><b>Checks:</b></p> <ul style="list-style-type: none"><li>• <a href="#">GRST</a> (Gated reset)</li><li>• <a href="#">MAX_LINES_PER_MODULE</a> (Long module/architecture)</li><li>• <a href="#">STATE_VAR_NAME</a> (Run name analysis on FSM state variable names)</li><li>• <a href="#">RSTMOD</a> (Report if internal resets exist)</li><li>• <a href="#">HCCC</a> (Do not hard-code constants)</li><li>• <a href="#">RANGE_CHECK</a> (Check range direction)</li><li>• <a href="#">UNCONNECTED_UNDRIVEN_UNUSED_NET</a> (Report unconnected undriven/unused signals)</li><li>• <a href="#">FSM_NO_HCCS</a> (FSM states do not use hard coded constants)</li><li>• <a href="#">DIFF_CLK_PROP_DFF_DATA</a> (Clock propagates to DFF data)</li><li>• <a href="#">MOS</a> (Mismatching operand size)</li><li>• <a href="#">NAME_ANALYSIS_CLOCKENABLE</a> (Report on clock enable names based on naming criteria)</li><li>• <a href="#">UNREACHABLE_STATE</a> (Report Unreachable states)</li><li>• <a href="#">UNCONNECTED_UNDRIVEN_UNUSED_PIN</a> (Report unconnected undriven/unused hierarchical instance pins)</li><li>• <a href="#">NAME_ANALYSIS_RESETS</a> (Report on reset names based on naming criteria)</li><li>• <a href="#">NO_INITIAL</a> (Don't use initial statements)</li><li>• <a href="#">MDA</a> (Missing case default assignment)</li><li>• <a href="#">LEC</a> (Little endian checks)</li><li>• <a href="#">CCLP</a> (0-count loops)</li><li>• <a href="#">INT_TRI</a> (Internal tristate objects)</li><li>• <a href="#">MULT_PORTS</a> (Multiple port declarations on same line)</li></ul>
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Check Selected    Uncheck Selected    Uncheck All    Reset to Default

다양한 종류의 Built-in Check 을 통한 Custom 한 검증 환경 제공

