Cryogenic computing, which runs computers at extremely low temperatures (e.g., 77K) has been emerged as a highly promising solution for the next-generation computing. To build the best cryogenic computer systems, architects should utilize the accurate performance model based on the cryogenic MOSFET and wire properties.

In this project, we fabricate MOSFET and wire samples with Samsung’s 65nm technology and measure their 77K properties to improve model’s accuracy. Next, we measure our samples’ $I_{ON}$ and wire resistance with the semiconductor analyze. We also compare our 65nm results with our previous 28nm measurements. Our analysis will greatly contribute to developing more accurate models for cryogenic computing.

**II. Design and Implementation**

Fig.1 shows the layout of the fabricated MOSFET and wire samples, which include 100 wire and 168 MOSFET samples with various wire length and gate width, respectively. For the wires, we fabricate ten types of wires whose wire lengths range from 90nm to 900nm, with the 90nm interval (W1 to W10). For the MOSFETs, we fabricate 12 types of samples whose gate widths range from 210nm to 2520nm with the 210nm interval (W1/P1 to W12/P12).

**III. Measurement result**

As shown in Fig.3(a) and Fig.3(b), we observed that the on-channel current (i.e., $I_{ON}$) slightly increases with the temperature reduction. For 65nm technology, $I_{ON}$ of NMOS and PMOS increases at 77K by 8.4% and 4.8% on average compared to the 300K value. On the other hand, in our previous measurement for 28nm technology, the $I_{ON}$ improvement is lower than that of 65nm technology (2.9% and -4.9% for NMOS and PMOS). In addition, we observe that gate width does not meaningfully affect the temperature dependency of $I_{ON}$ with 4.4% and 6.6% of maximum difference on 77K-to-300K ratio for 65nm technology.

**IV. Conclusion**

In this project, we measured and analyzed 65nm technology node's MOSFET and wire characteristics at 77K, to build more accurate cryogenic MOSFET and wire models. We observe the slightly higher $I_{ON}$ for both NMOS and PMOS, and significantly reduced wire resistance at 77K.